LISTING OF THE CLAIMS (1-31)

Claim 1 (canceled)

Claim 2 (previously presented): The MIS device of Claim 4, further comprising a gate adjacent to said first insulative layer and said second insulative layer within said trench.

C1

Claim 3. (Previously presented): The MIS device of Claim 2, wherein said gate comprises polysilicon.

Claim 4 (previously presented): A metal-insulator-semiconductor (MIS) device, comprising:

a semiconductor substrate defining a trench extending into said substrate from a surface of said substrate;

a source region of a first conductivity type adjacent to a sidewall of said trench and to said surface;

a body region of a second conductivity type opposite to said first conductivity type adjacent to said source region and to said sidewall;

a drain region of said first conductivity type adjacent to said body region and to said sidewall;

wherein said trench is lined with a first insulative layer along a portion of said sidewall that abuts said body region and wherein said trench is lined with a second deposited insulated layer along said bottom portion of said trench, said second insulative layer being in contact with said first insulative layer, whereby formation of said second insulative layer does not introduce substantial stress in said substrate; and

a ~~high conductivity~~highly doped region of said first conductivity type in said drain region ~~adjacent to at least~~in contact with said bottom portion of said trench.

Claim 5 (previously presented): The MIS device of Claim 4, wherein said first insulative layer comprises an oxide.

Claim 6 (previously presented): The MIS device of Claim 4, wherein said second insulative layer comprises an oxide.

Claim 7 (previously presented): The MIS device of Claim 4,wherein said second insulative layer is a multi-layer insulative layer.

Claim 8 (previously presented): The MIS device of Claim 4, wherein said MIS device is a MOSFET.

Claim 9 (canceled)

Claim 10 (previously presented): The trench-gate device of Claim 11, wherein said gate comprises polysilicon.

Claim 11 (previously presented): A trench-gate device, comprising:

a semiconductor substrate defining a trench extending into said substrate from a surface of said substrate;

a source region of a first conductivity type adjacent to a sidewall of said trench and to said surface;

a body region of a second conductivity type opposite to said first conductivity type adjacent to said source region and to said sidewall;

a drain region of said first conductivity type adjacent to said body region and to said sidewall;

wherein said trench is lined with a first insulative layer along a portion of said sidewall that abuts said body region and wherein said trench is lined with a second deposited insulated layer along said bottom portion of said trench, said second insulative layer being in contact with said first insulative layer and said second insulative layer being thicker than said first insulative layer whereby formation of said second insulative layer does not introduce substantial stress in said substrate;

a gate adjacent to said first insulative layer and said second insulative layer within said trench; and

a ~~high conductivity~~highly doped region of said first conductivity type in said drain region ~~adjacent to at least~~in contact with said bottom portion of said trench.

Claim 12 (previously presented): The trench-gate device of Claim 11, wherein said first insulative layer comprises an oxide.

Claim 13 (previously presented): The trench-gate device of Claim 11, wherein said second insulative layer comprises an oxide.

Claim 14 (previously presented): The trench-gate device of Claim 11, wherein said second insulative layer is a multi-layer insulative layer.

Claim 15 (canceled)

Claim 16 (previously presented) A trench-gate device, comprising:
a semiconductor substrate defining a trench extending into said substrate from a surface of said substrate;
a source region of a first conductivity type adjacent to a sidewall of said trench and to said surface;
a body region of a second conductivity type opposite to said first conductivity type adjacent to said source region and to said sidewall;
a drain region of said first conductivity type adjacent to said body region and to said sidewall;
a first insulative layer lining said trench along a portion of said sidewall that abuts said body region;
a second deposited insulated layer lining said trench along a bottom portion of said trench, said second insulative layer being thicker than said first insulative layer and said second insulative layer being in contact with said first insulative layer;
wherein a thickness of a transition insulative layer at the juncture of said first insulative layer and said second insulative layer is not less than a thickness of said first insulative layer;
a gate adjacent to said first insulative layer and said second insulative layer within said trench; and
a ~~high conductivity~~highly doped region of said first conductivity type in said drain region ~~adjacent to at least~~in contact with said bottom portion of said trench.

Cl cont.

Claim 17 (canceled)

Claim 18 (previously presented): A trench-gate device, comprising:
a semiconductor substrate defining a trench extending into said substrate from a surface of said substrate;
a source region of a first conductivity type adjacent to a sidewall of said trench and to said surface;
a body region of a second conductivity type opposite to said first conductivity type adjacent to said source region and to said sidewall;
a drain region of said first conductivity type adjacent to said body region and to said sidewall;
a first insulative layer lining said trench along a portion of said sidewall that abuts said body region;

a second deposited insulated layer lining said trench along a bottom portion of said trench, said second insulative layer being thicker than said first insulative layer and said second insulative layer being in contact with said first insulative layer, whereby formation of said second insulative layer does not introduce substantial stress into said substrate;

wherein a width of said trench at a vertical midpoint of said second insulative layer is not greater than a width of said trench adjacent to said body region;

C1 a gate adjacent to said first insulative layer and said second insulative layer within said trench; and

a ~~high conductivity~~highly doped region of said first conductivity type in said drain region ~~adjacent to at least~~in contact with said bottom portion of said trench.

Claims 19-29 (canceled)

Claim 30 (previously presented): The MIS device of Claim 4, wherein the first insulative layer is thermally grown.

Claim 31 (previously presented): The trench-gate device of Claim 11, wherein the first insulative layer is thermally grown.